

FIG. 1

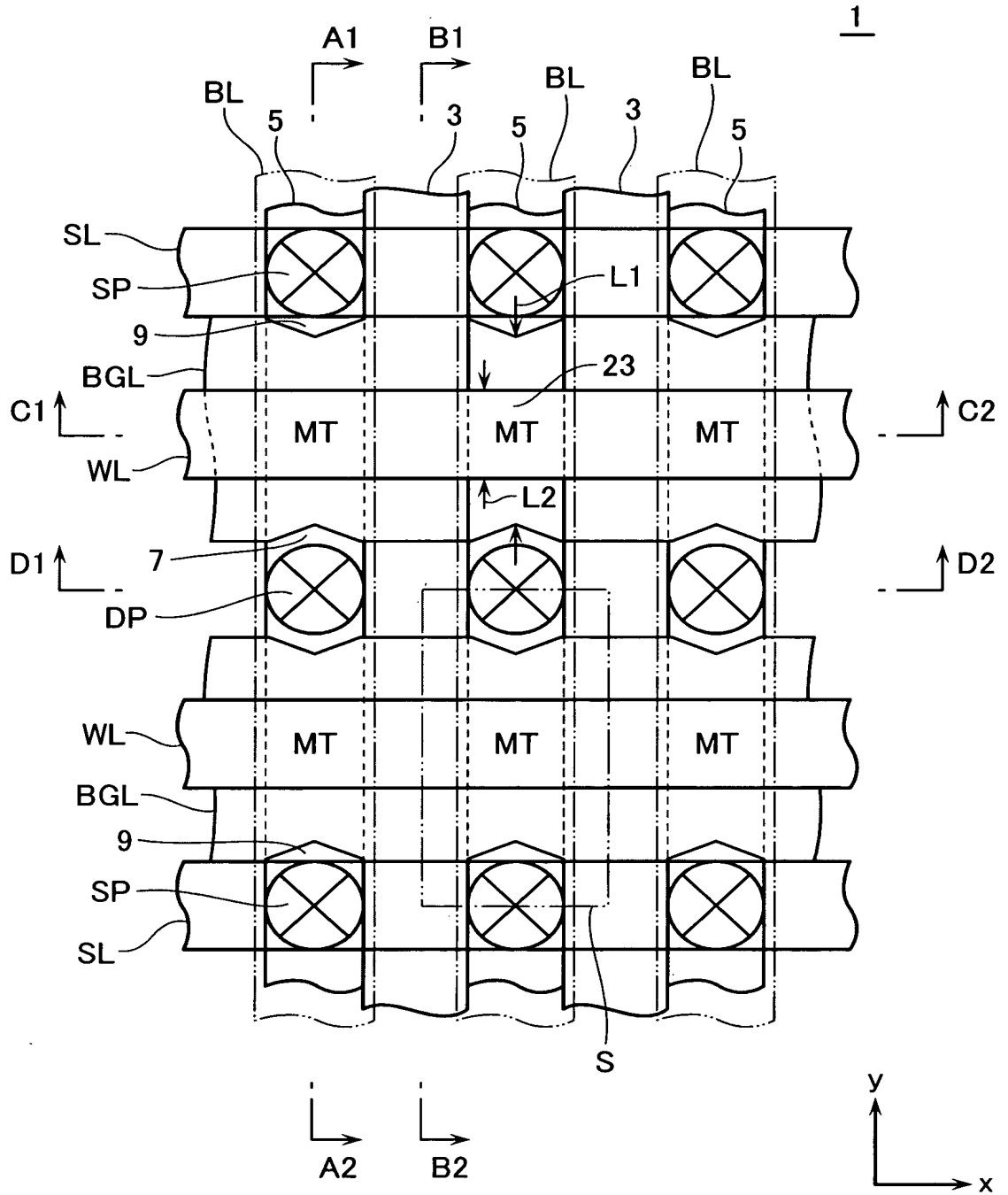




FIG. 2C

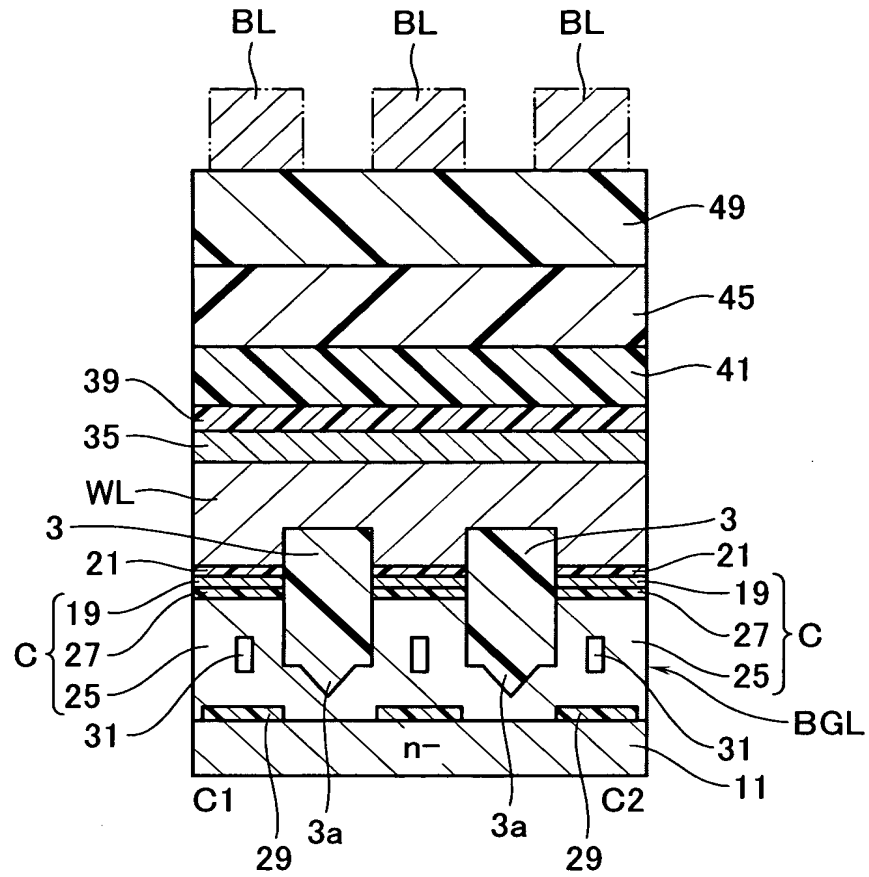


FIG. 2D

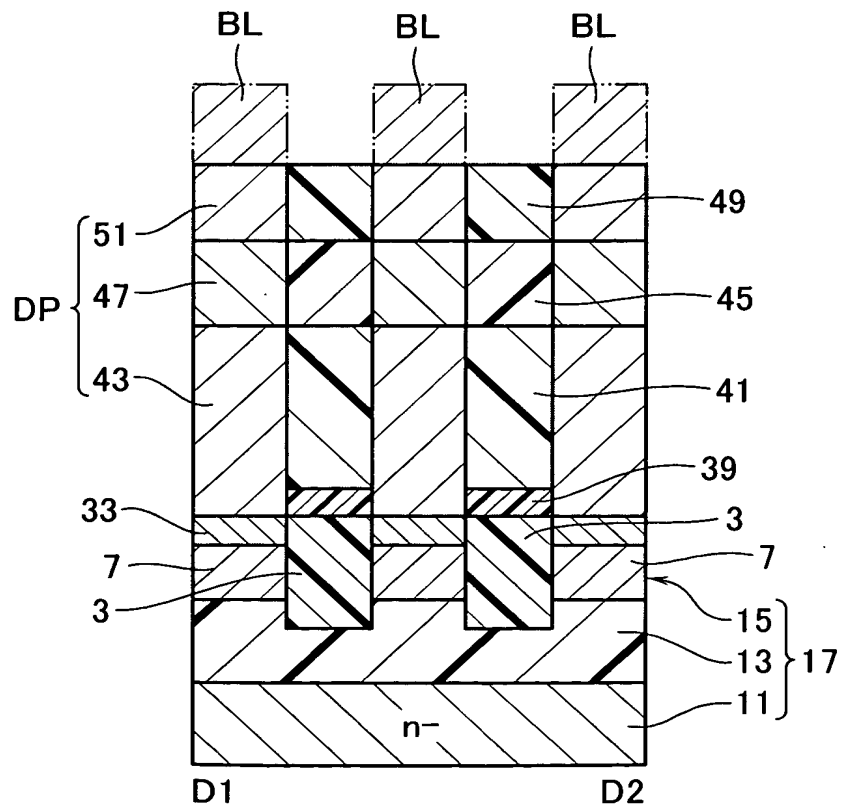


FIG. 3

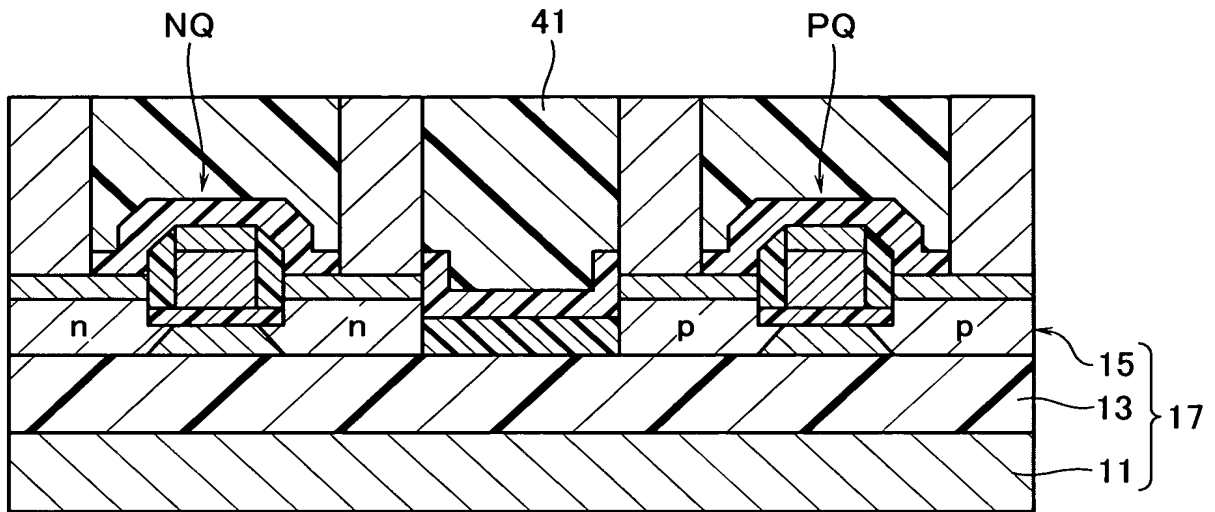


FIG. 4

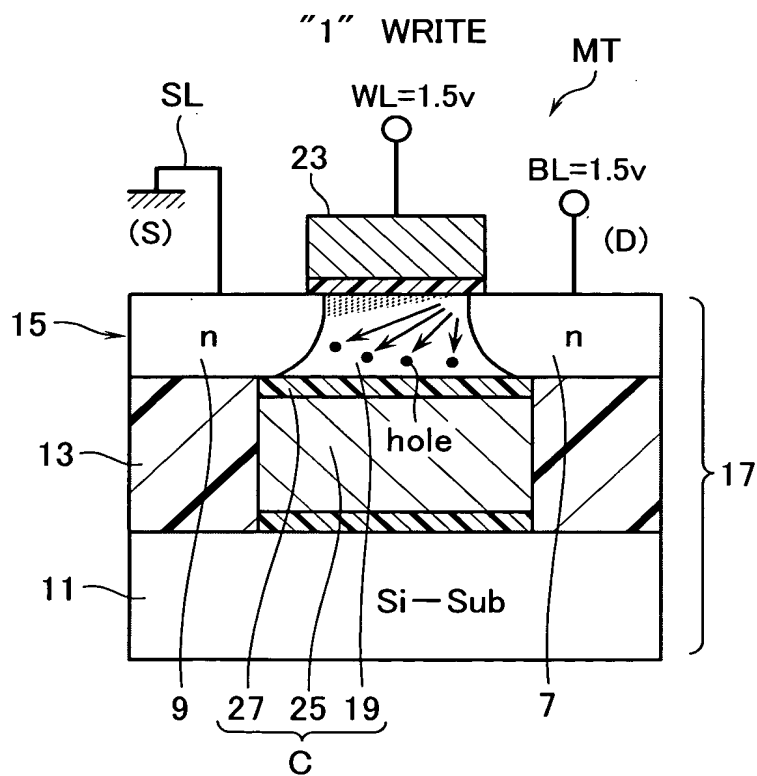


FIG. 5

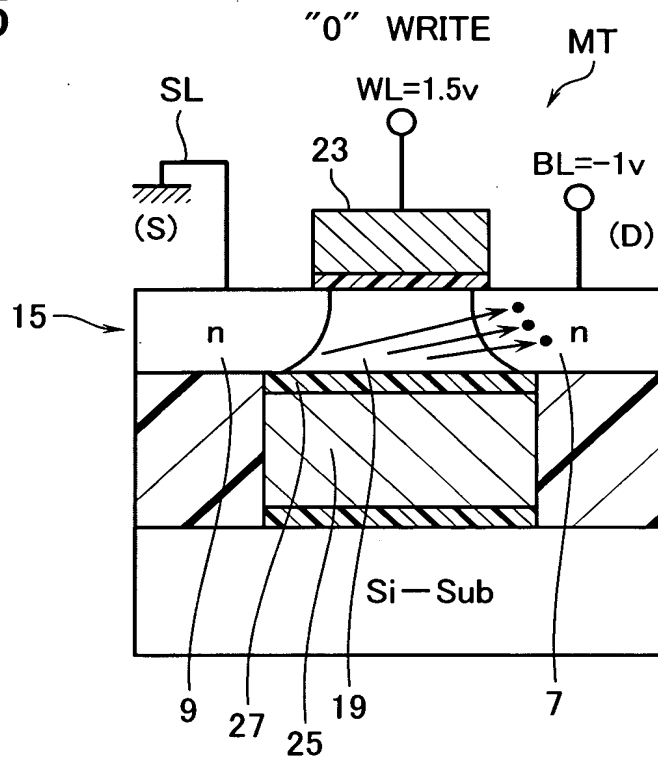


FIG. 6

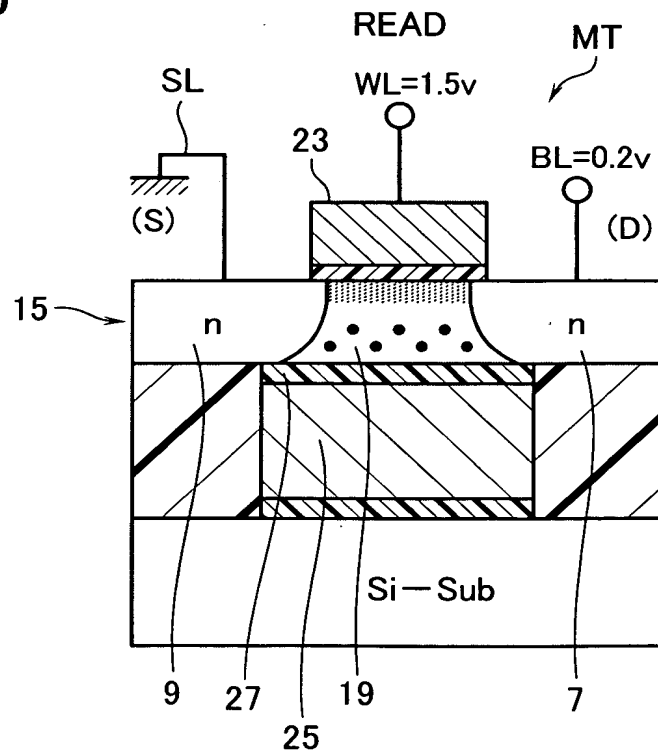


FIG. 7

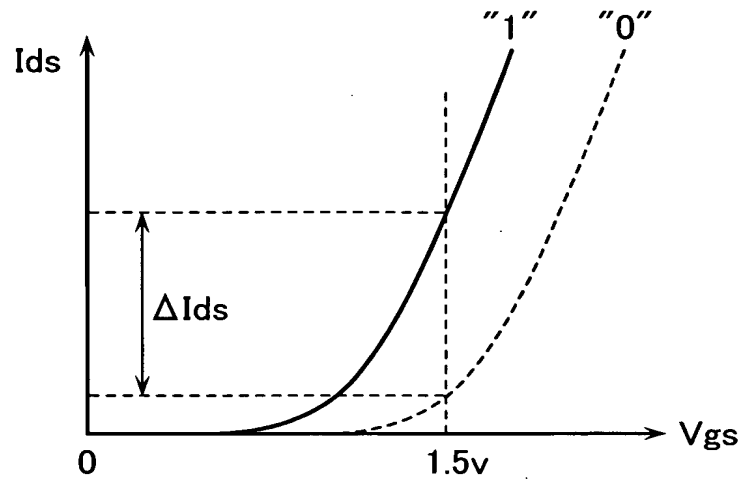


FIG. 8

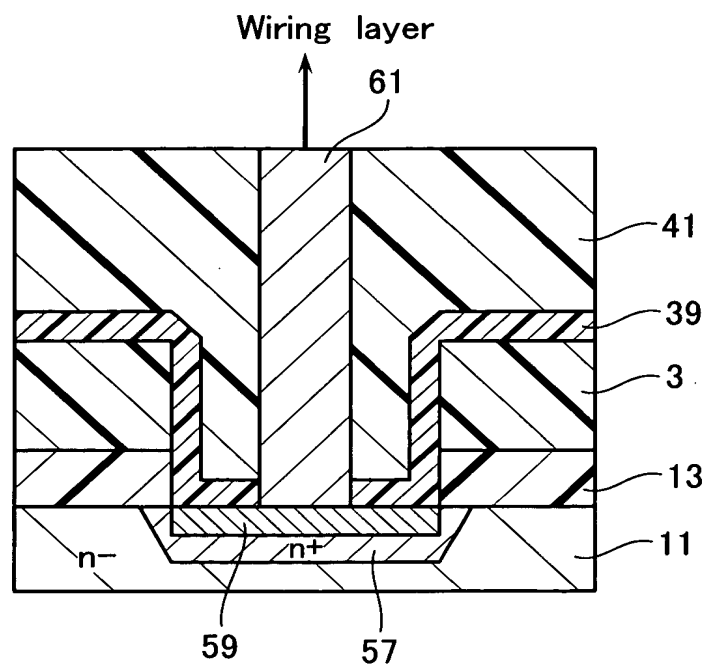


FIG. 9

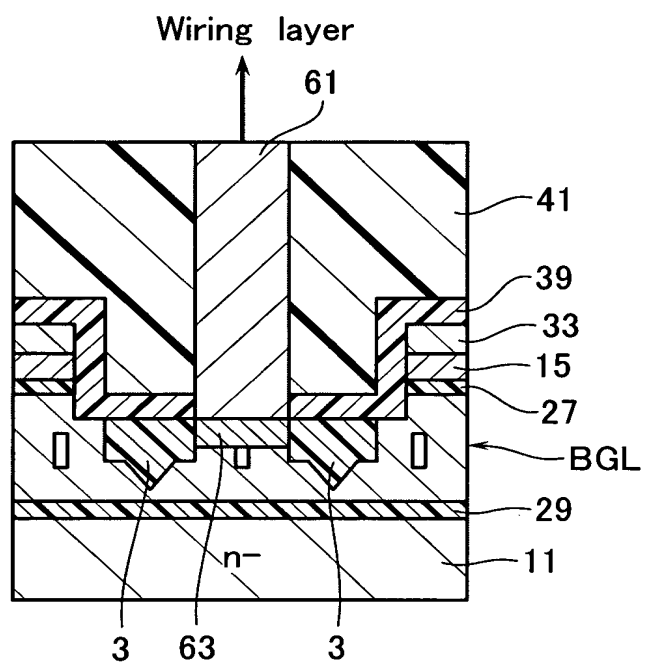


FIG. 10

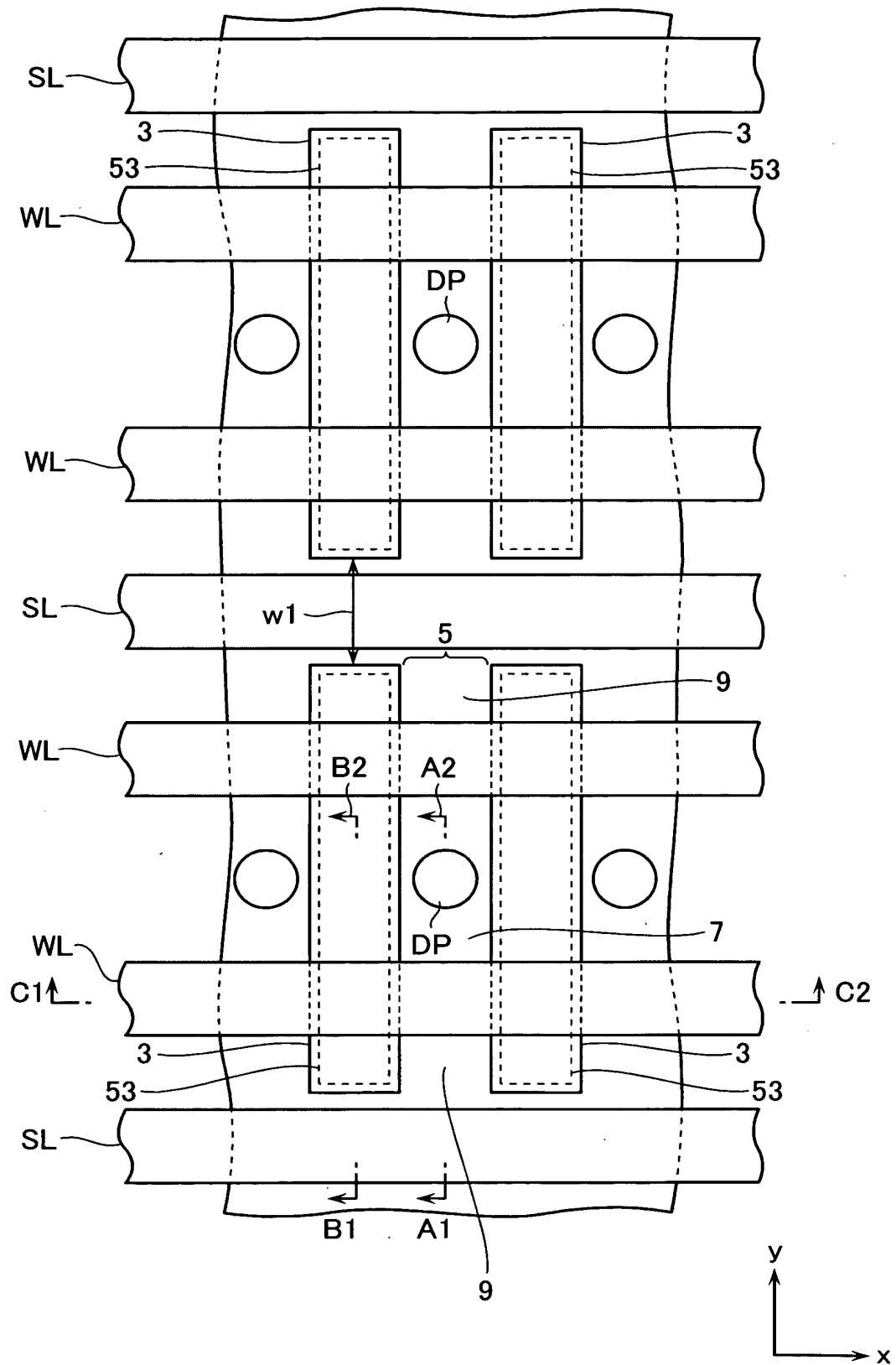




FIG. 11

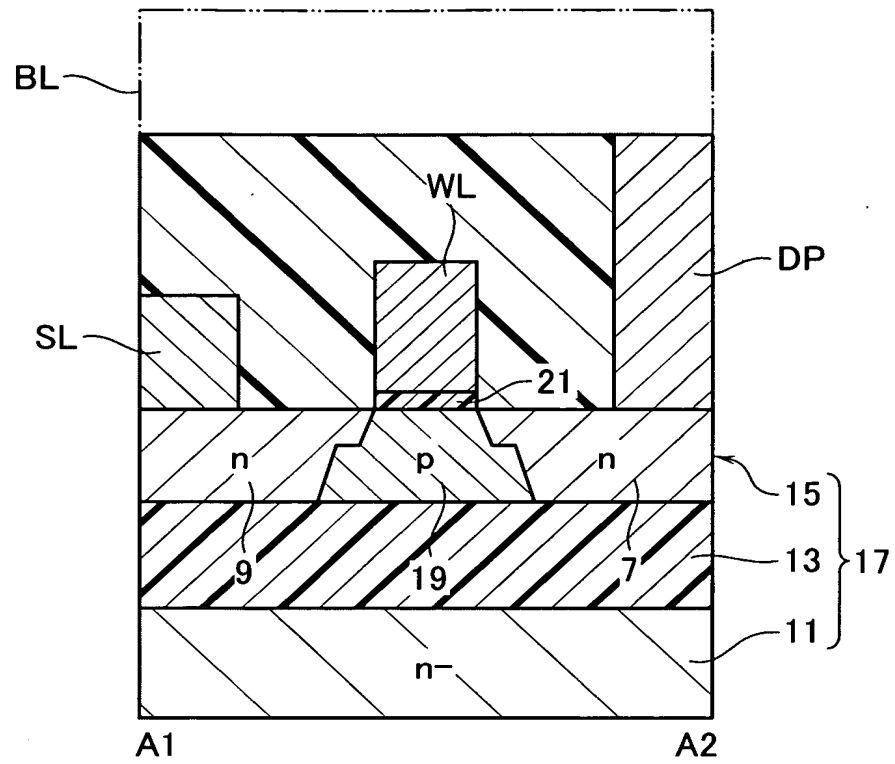


FIG. 12

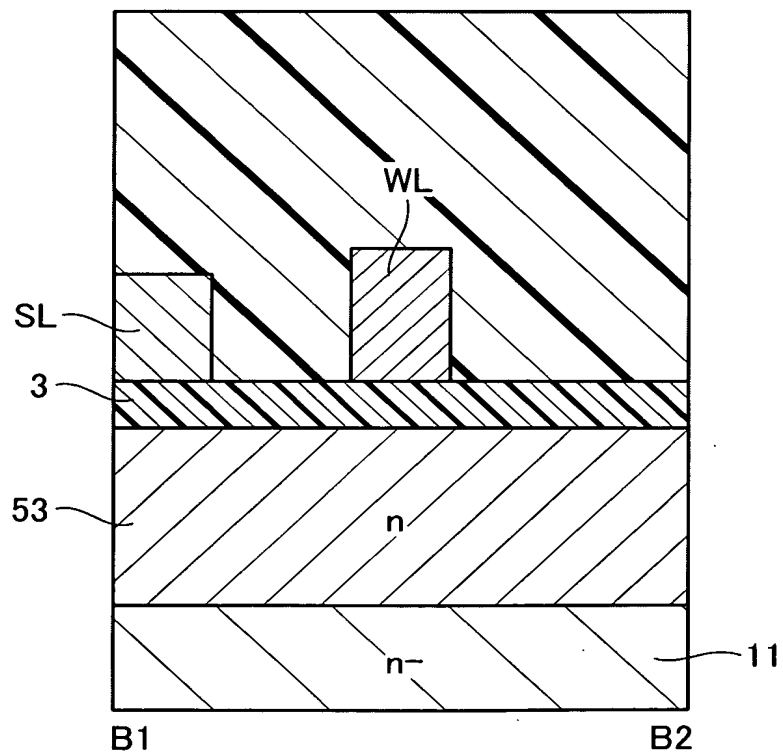


FIG. 13

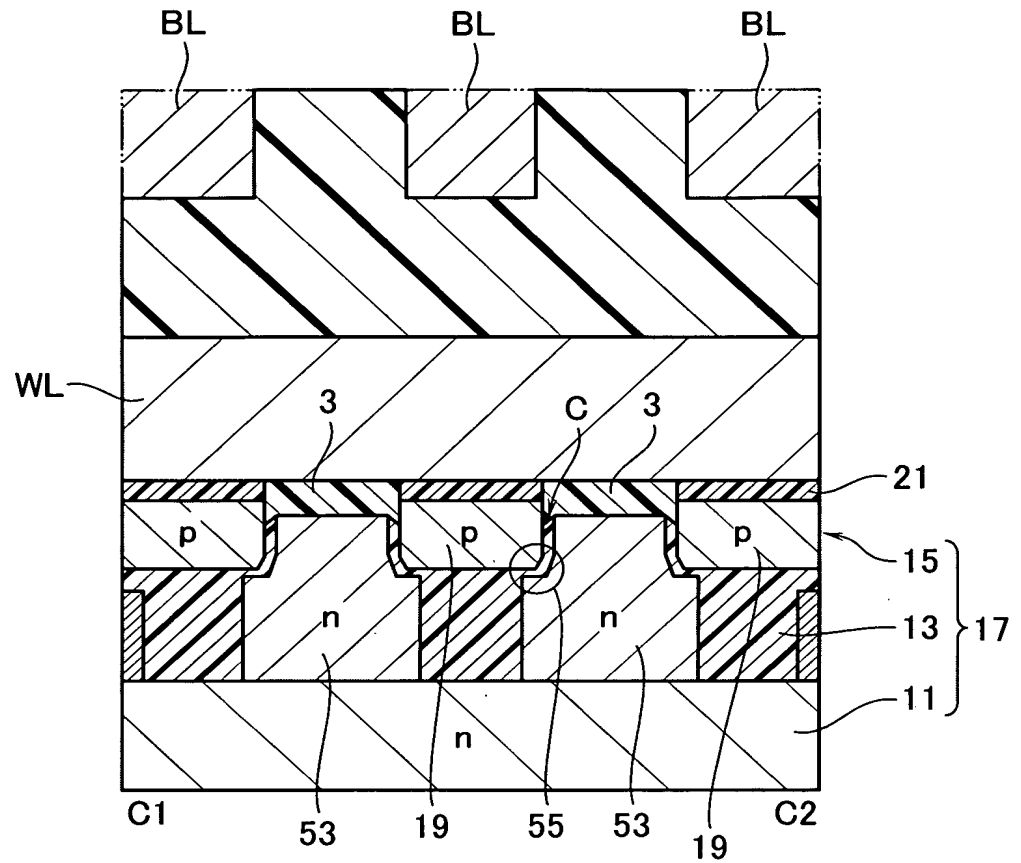


FIG. 14

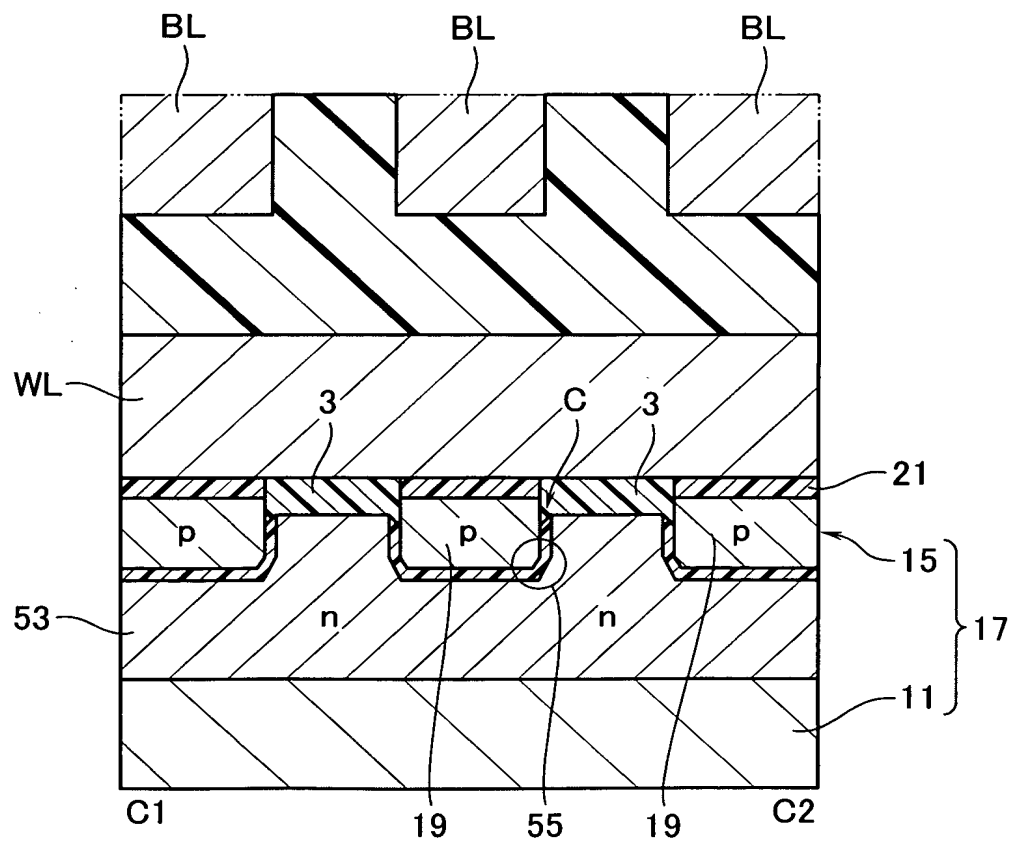


FIG. 15A

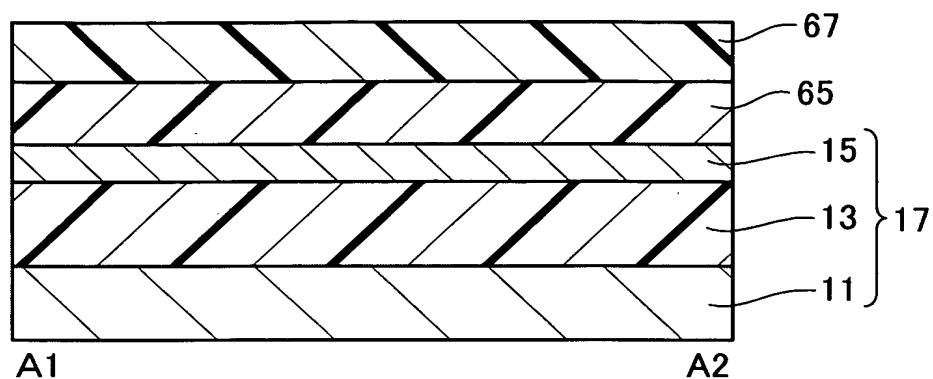


FIG. 15B

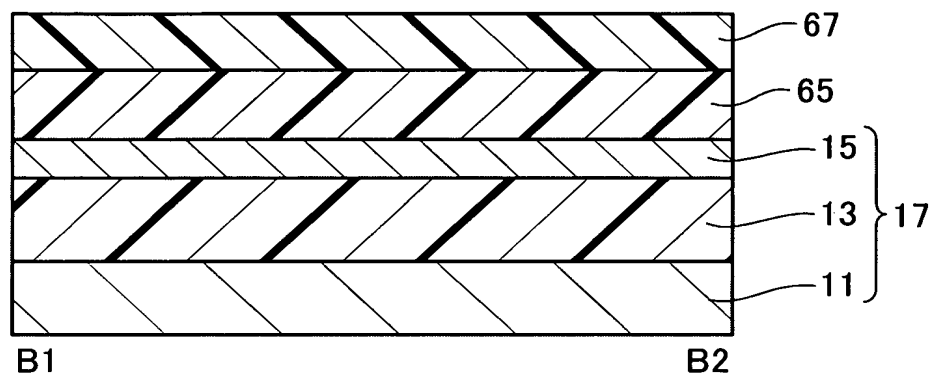


FIG. 15C

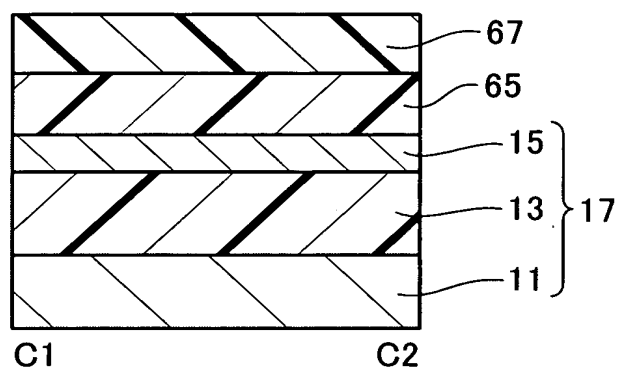


FIG. 15D

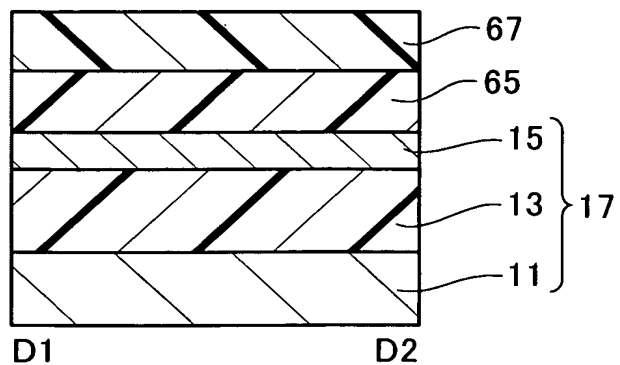


FIG. 16A

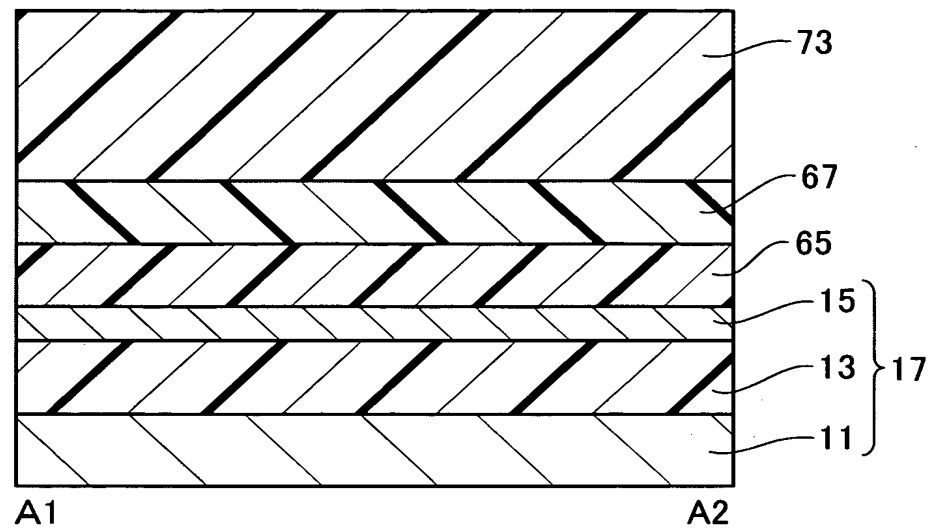


FIG. 16B

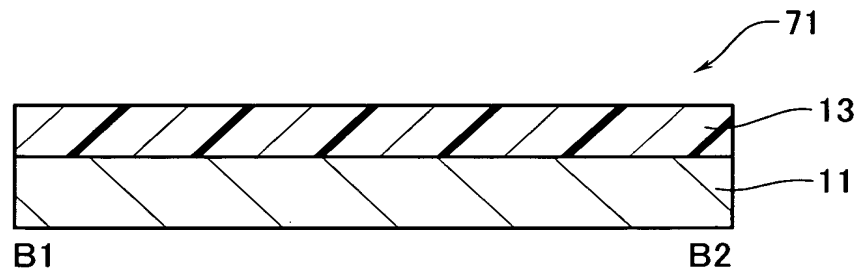


Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 11 with a base layer 13 and a patterned layer 15. A central region 69 is defined by a top layer 71 and a bottom layer 73. The device is labeled C1 and C2.

A cross-sectional view of a semiconductor device. It features a U-shaped structure with three vertical pillars. The left and right pillars are filled with a material having diagonal hatching. The central pillar is empty. The base of the structure is a horizontal layer. Labels include: 69 (top of the central pillar), 71 (left side of the central pillar), 73 (right side of the central pillar), 67 (top of the right pillar), 65 (middle of the right pillar), 15 (bottom of the right pillar), 13 (bottom of the right pillar), 11 (bottom of the right pillar), 17 (bottom of the right pillar), D1 (bottom left), and D2 (bottom right).

FIG. 17A

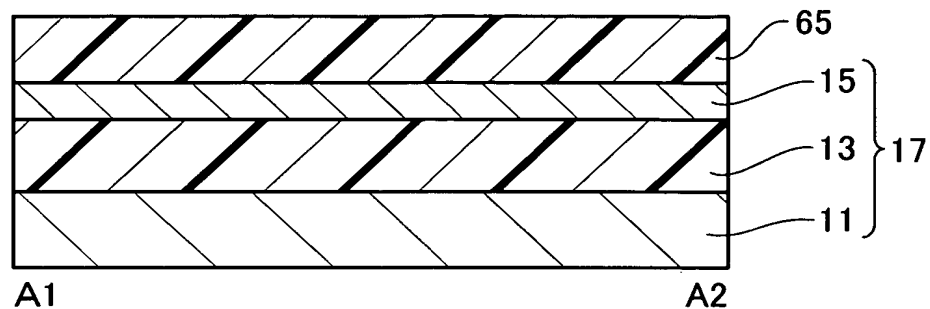


FIG. 17B

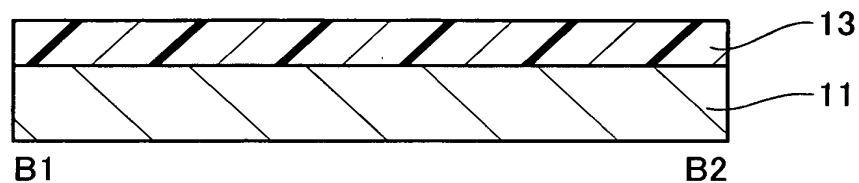


FIG. 17C

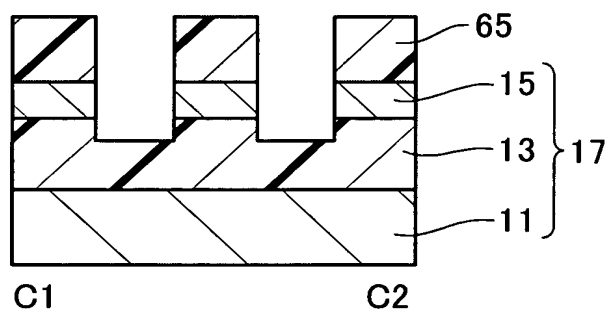


FIG. 17D

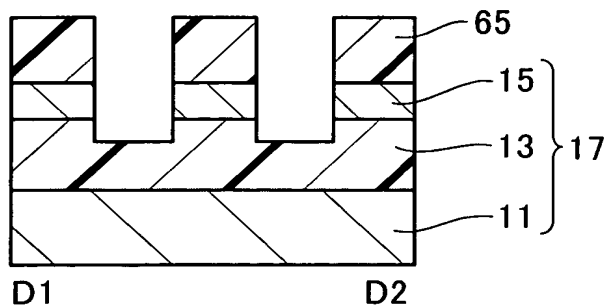


FIG. 18A

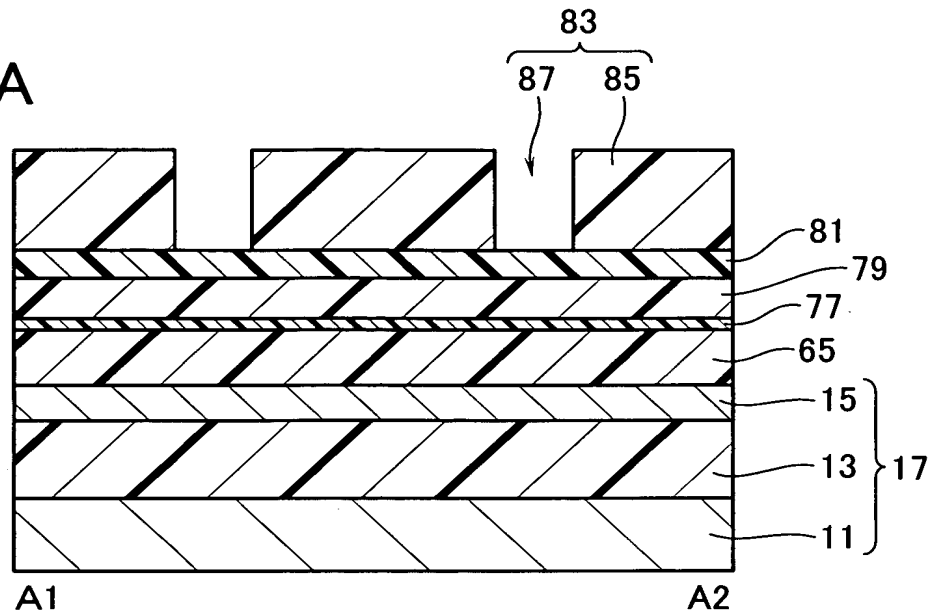


FIG. 18B

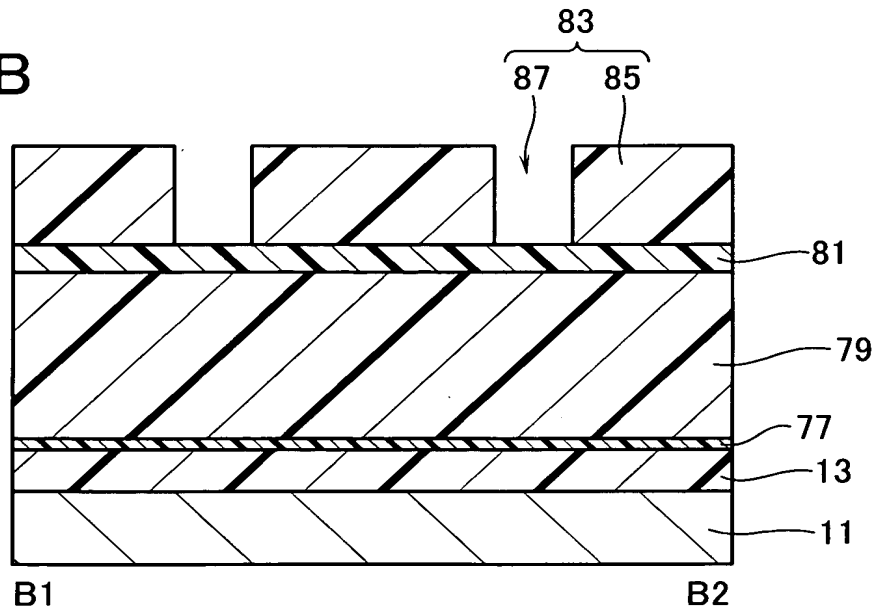


FIG. 18C

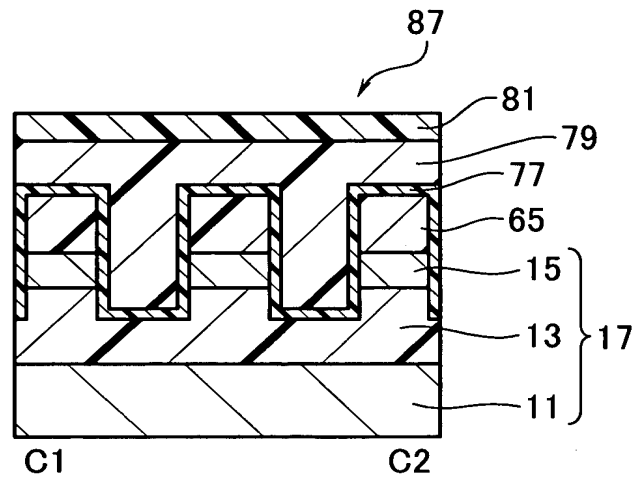


FIG. 18D

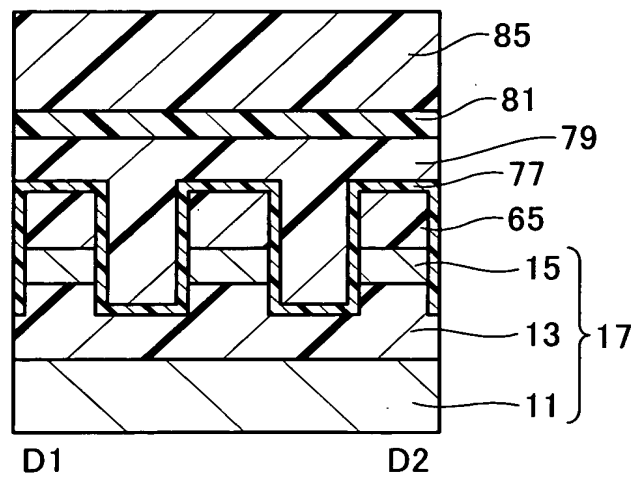




FIG. 19A

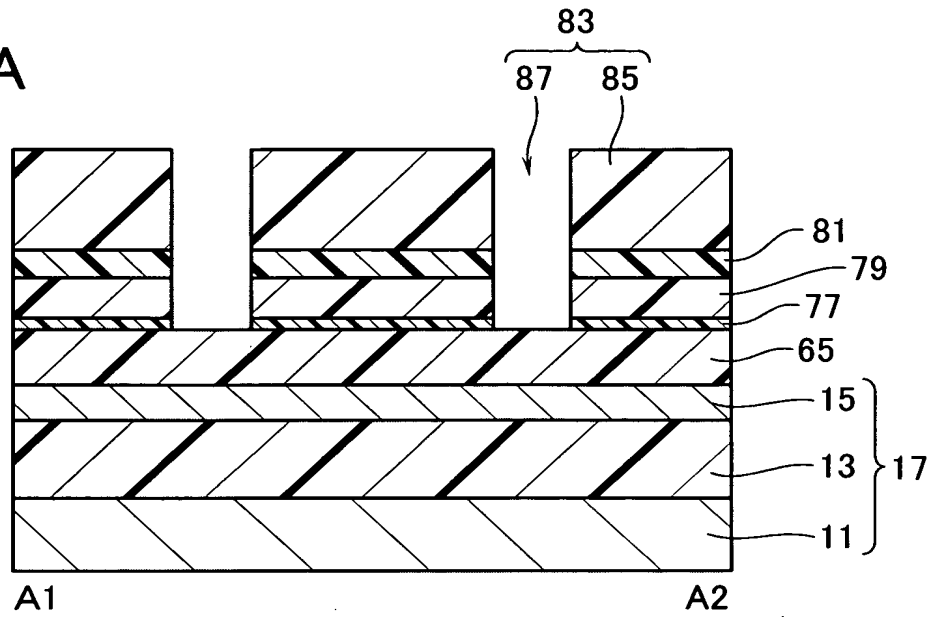


FIG. 19B

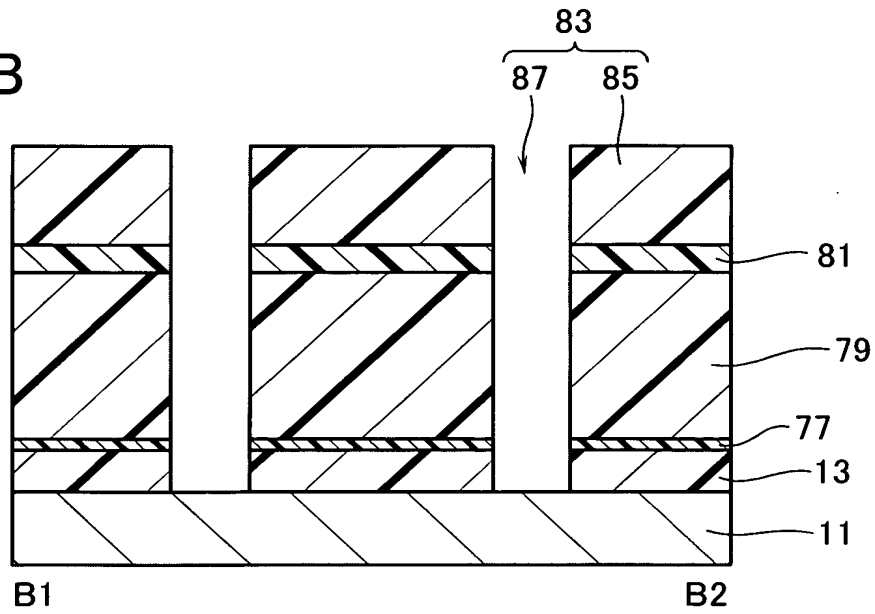


FIG. 19C

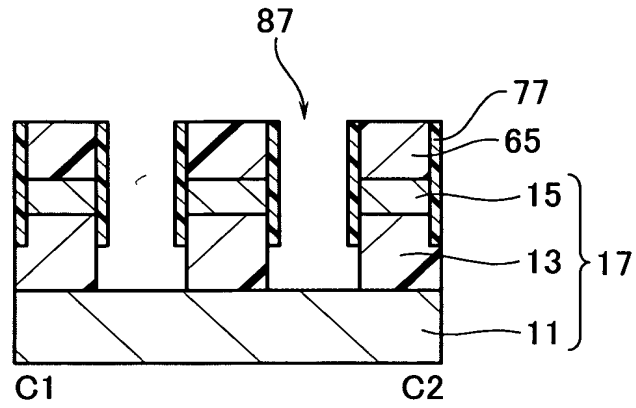


FIG. 19D

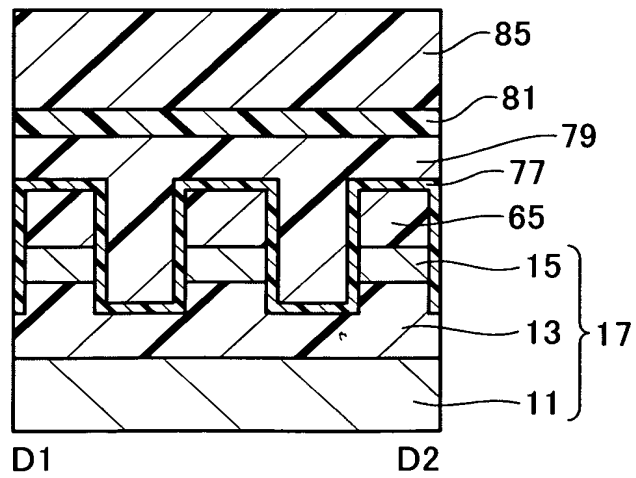


FIG. 20A

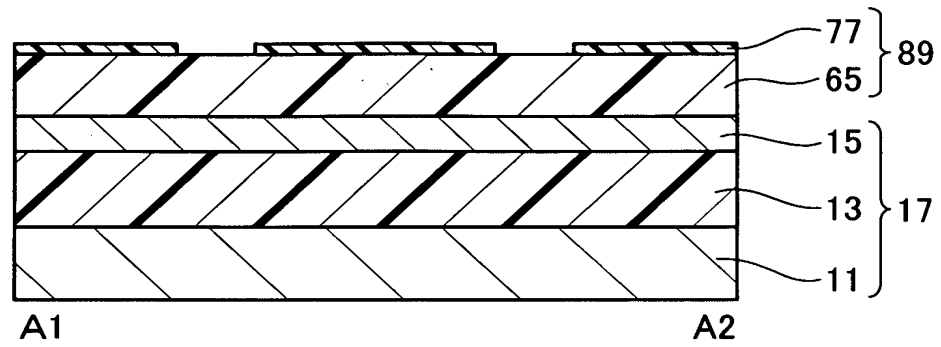


FIG. 20B

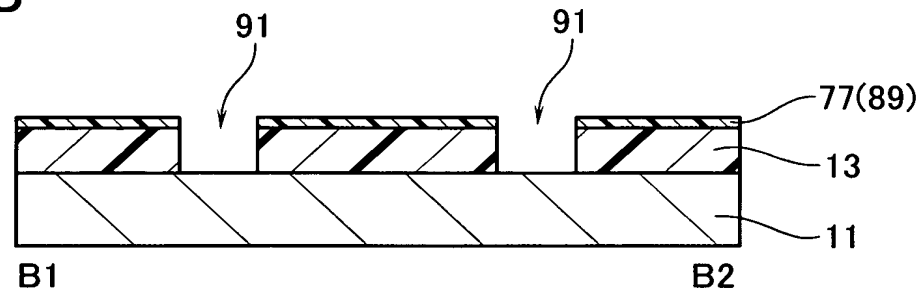


FIG. 20C

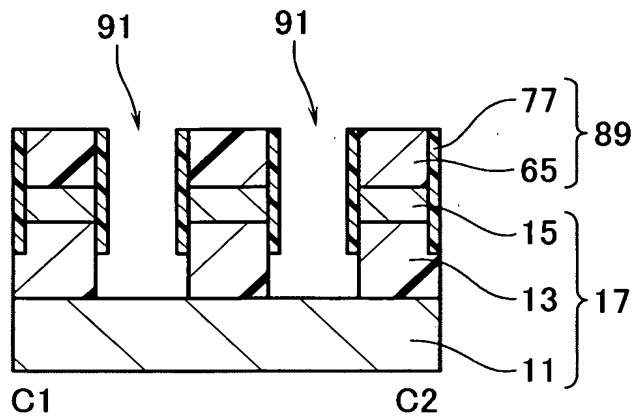


FIG. 20D

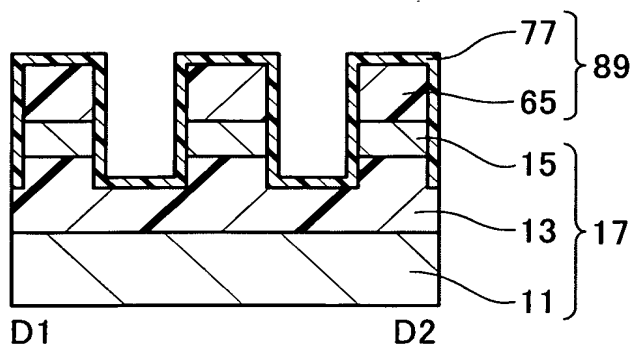




FIG. 22A

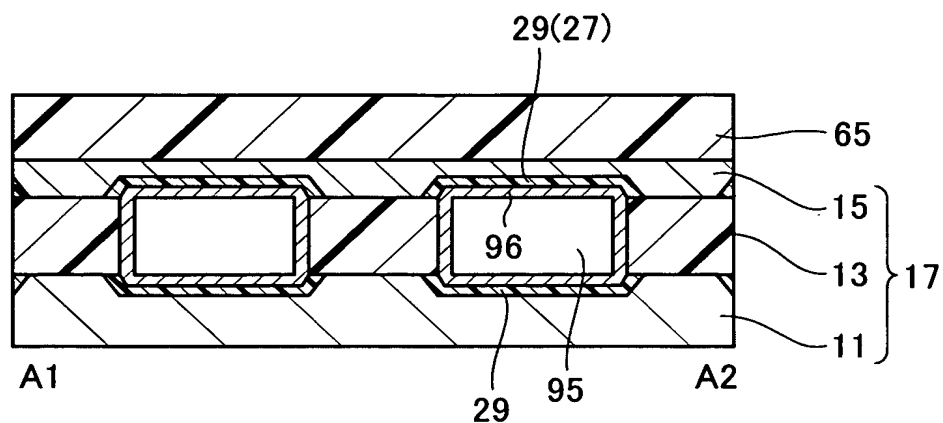


FIG. 22B

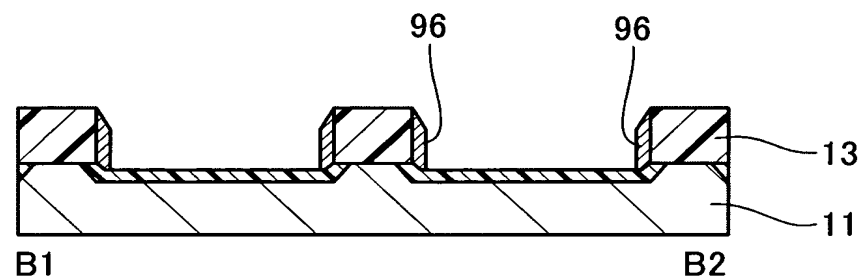


FIG. 22C

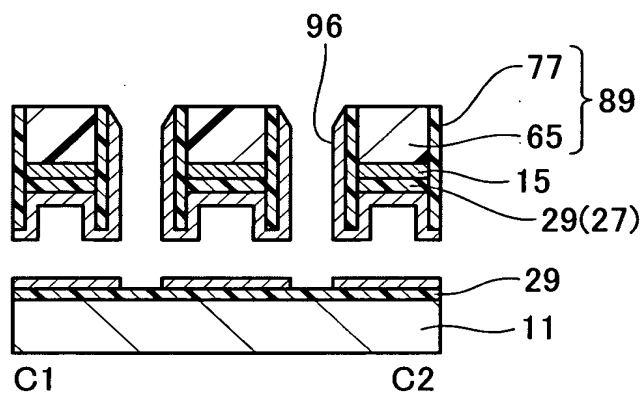


FIG. 22D

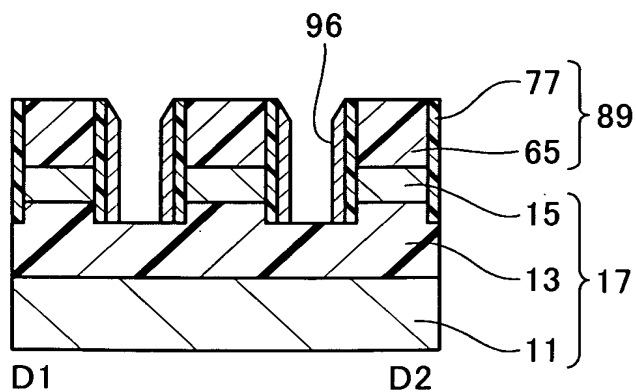


FIG. 23A

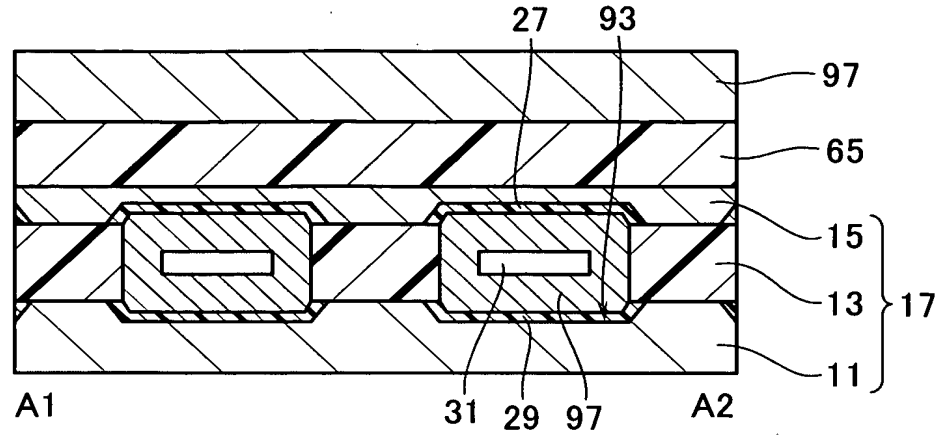


FIG. 23B

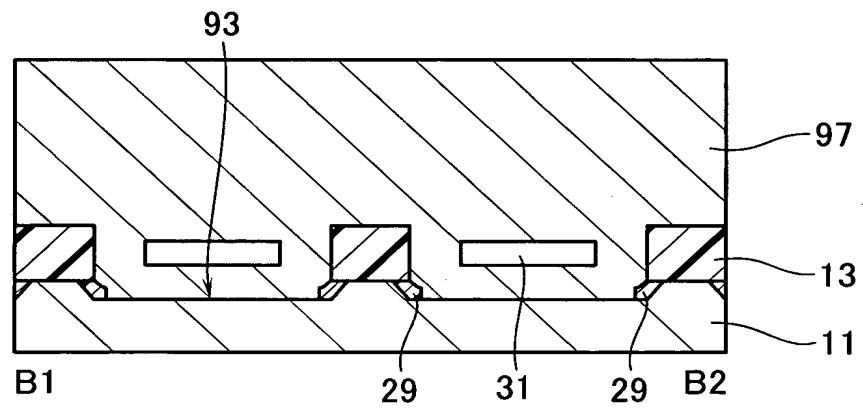


FIG. 23C

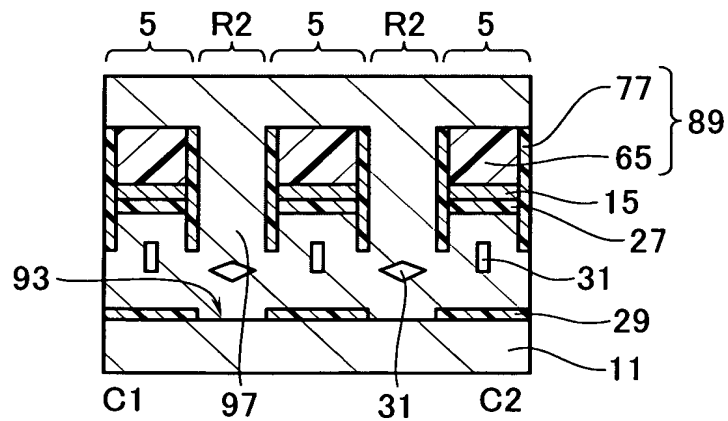


FIG. 23D

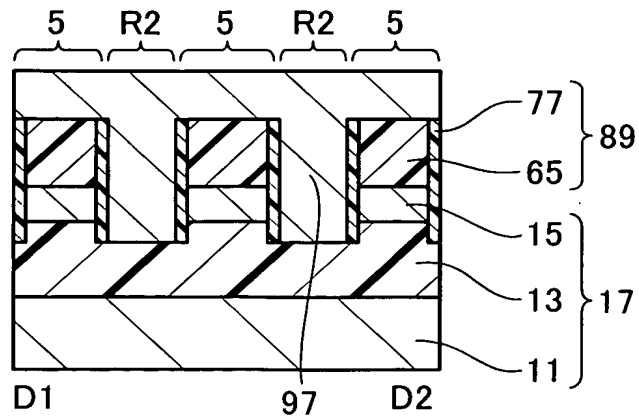


FIG. 24A

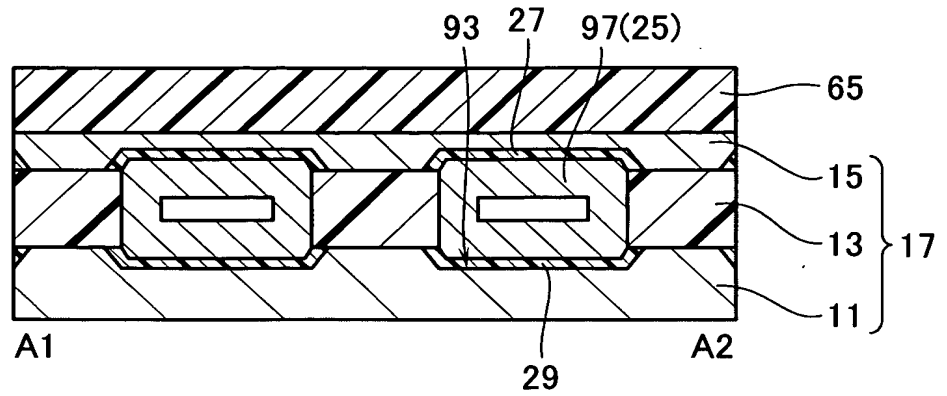


FIG. 24B

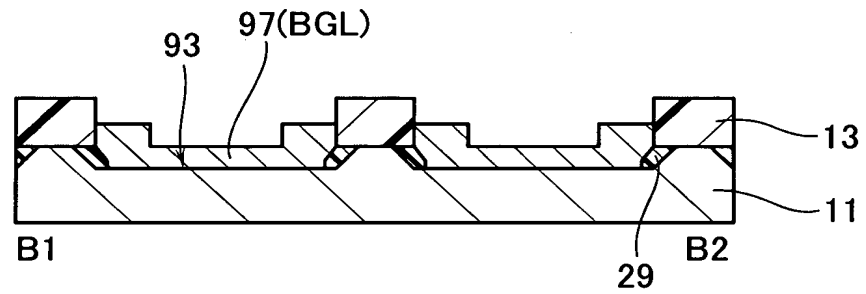


FIG. 24C

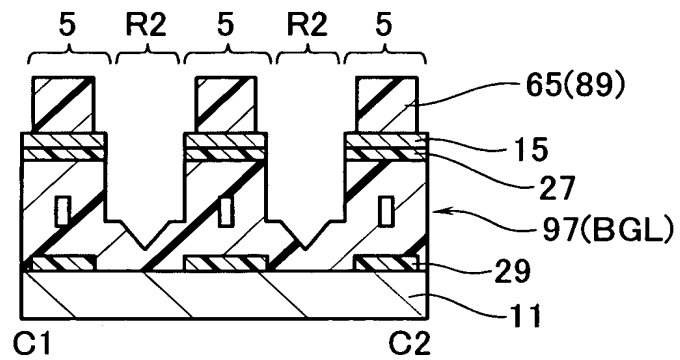
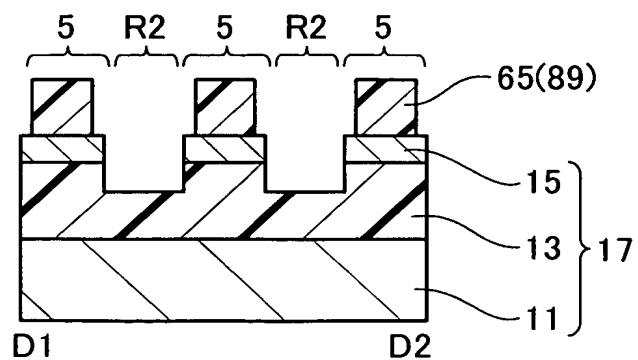


FIG. 24D





A cross-sectional view of a multi-layered structure. The structure consists of several horizontal layers. The top layer is labeled 99. Below it is a layer labeled 65. The bottom layer is labeled 11. In the center, there are two rectangular components, each labeled 15. These components are embedded within a layer labeled 13. The components 15 are connected by a horizontal line labeled 29. The entire assembly is bounded by vertical lines labeled A1 and A2. Other labels include 93, 27, and 25, which point to specific features within the layers.

Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 11, a layer 13, and a series of rectangular blocks 15. Each block 15 contains a square region 65. A thick layer 99 is formed on top of the blocks 15. The device is labeled D1 and D2 at the bottom corners.

FIG. 26A

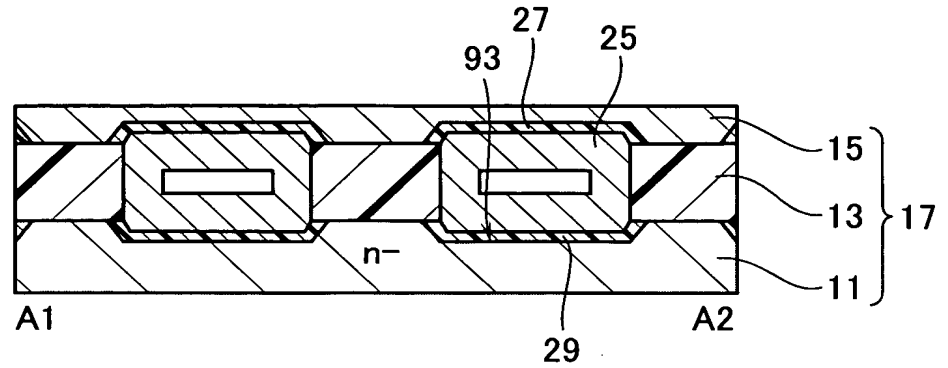


FIG. 26B

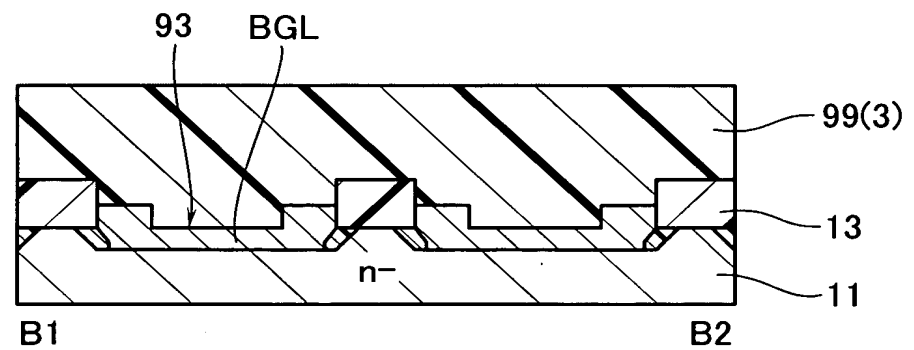


FIG. 26C

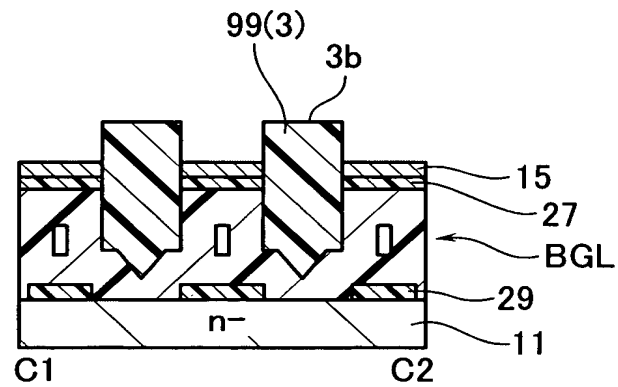


FIG. 26D

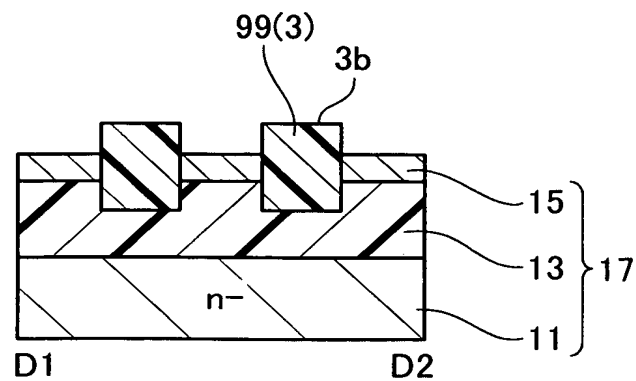


FIG. 27

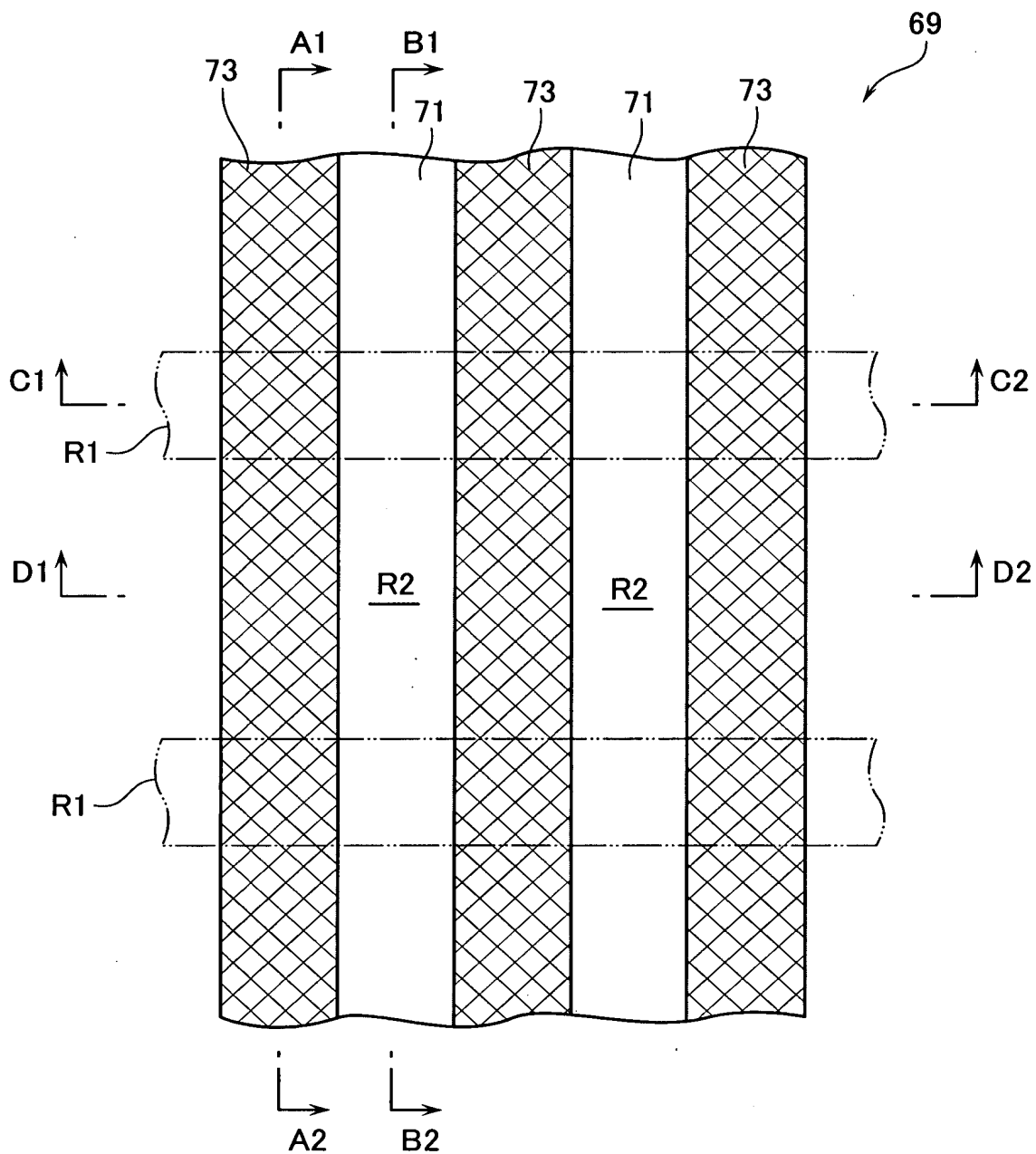


FIG. 28

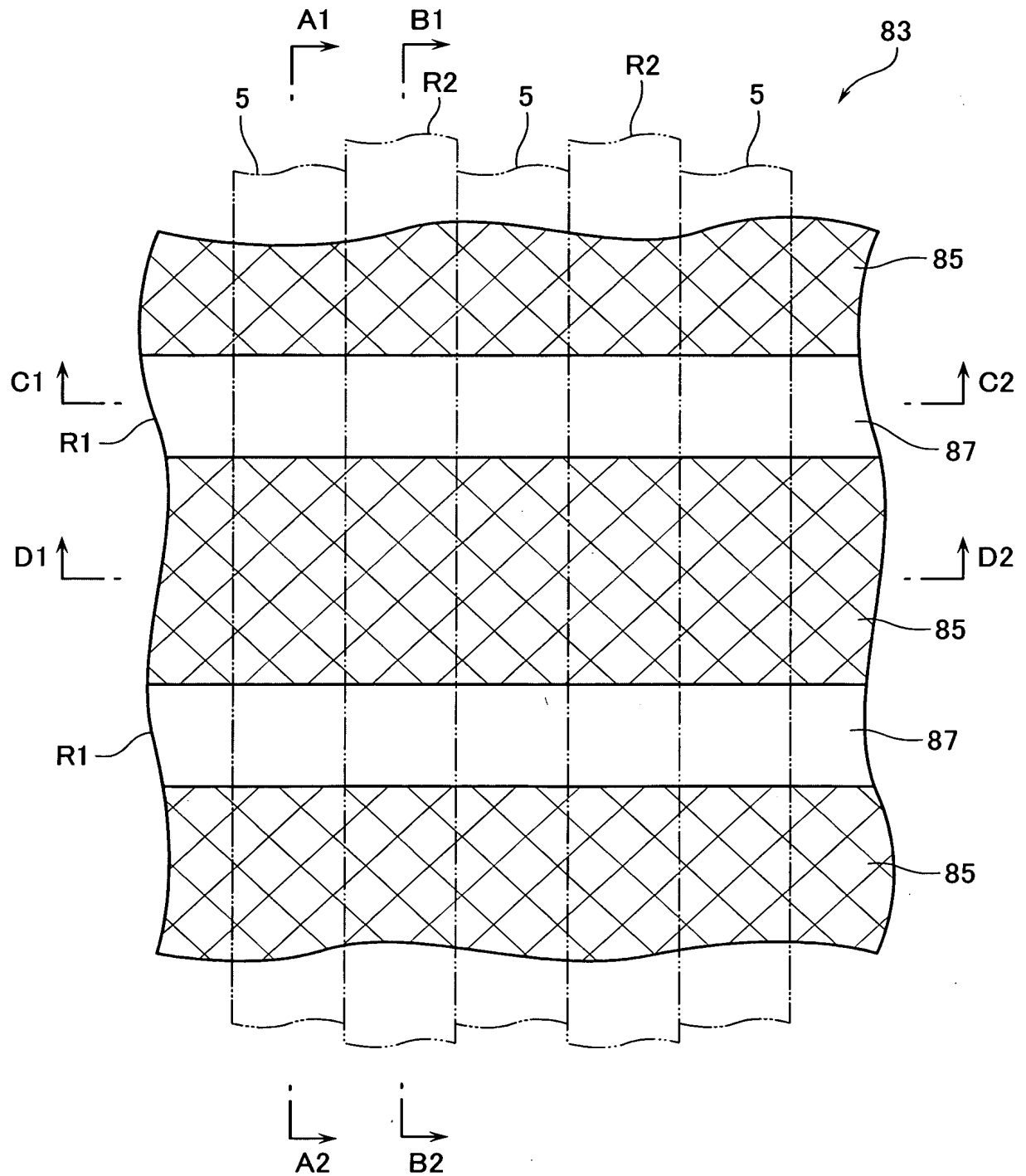


FIG. 29

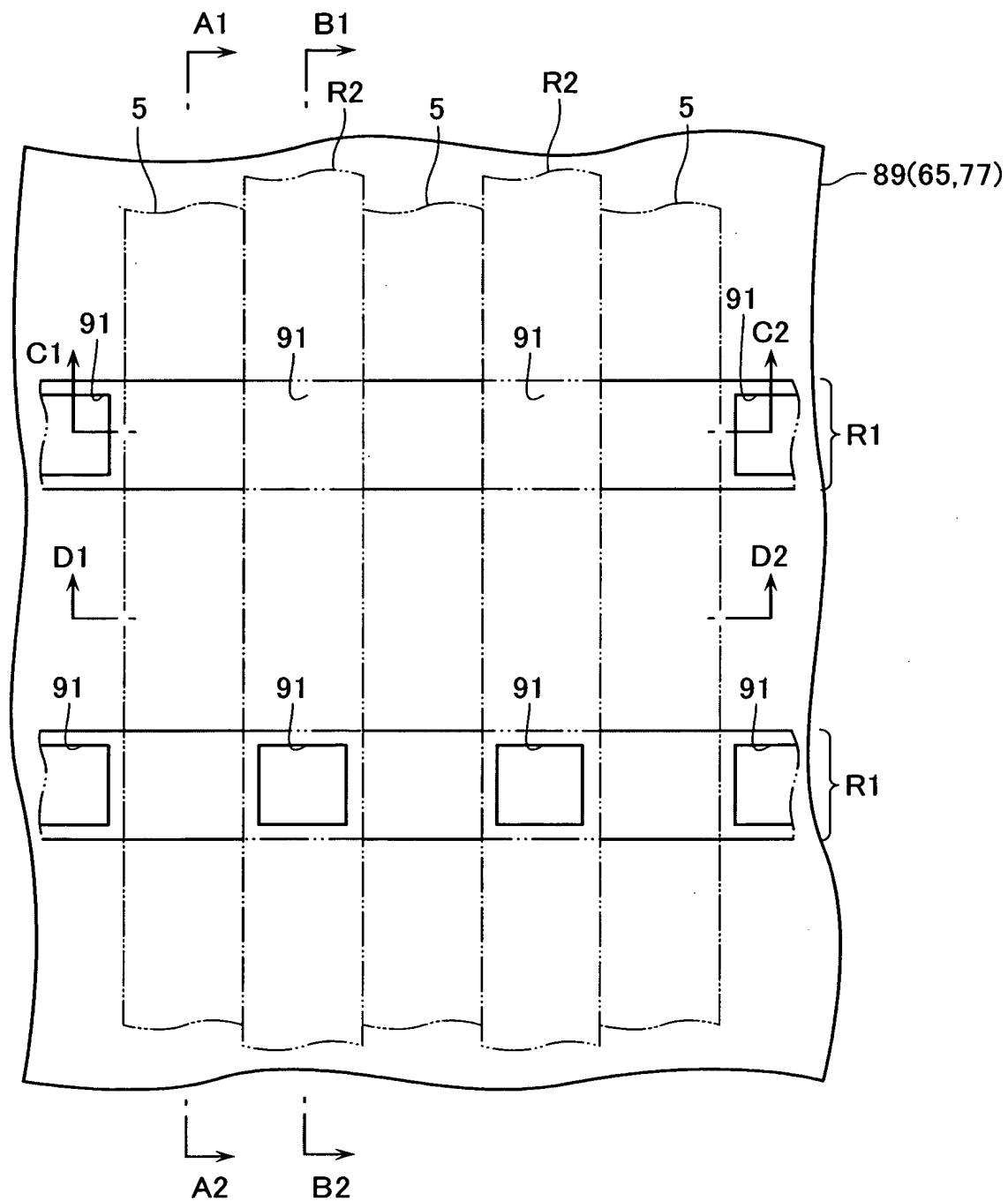


FIG. 30

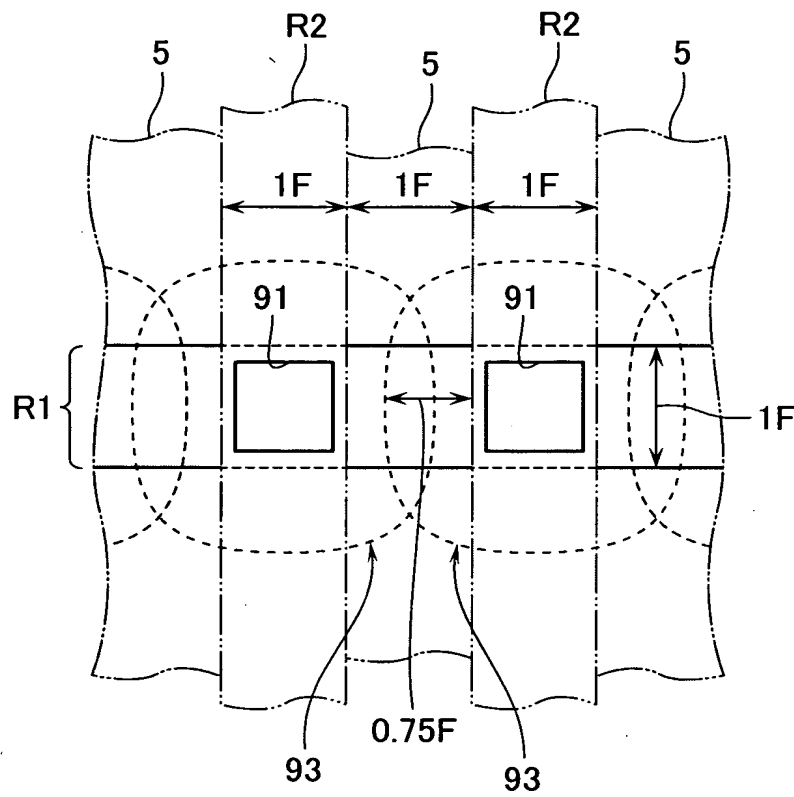


FIG. 31

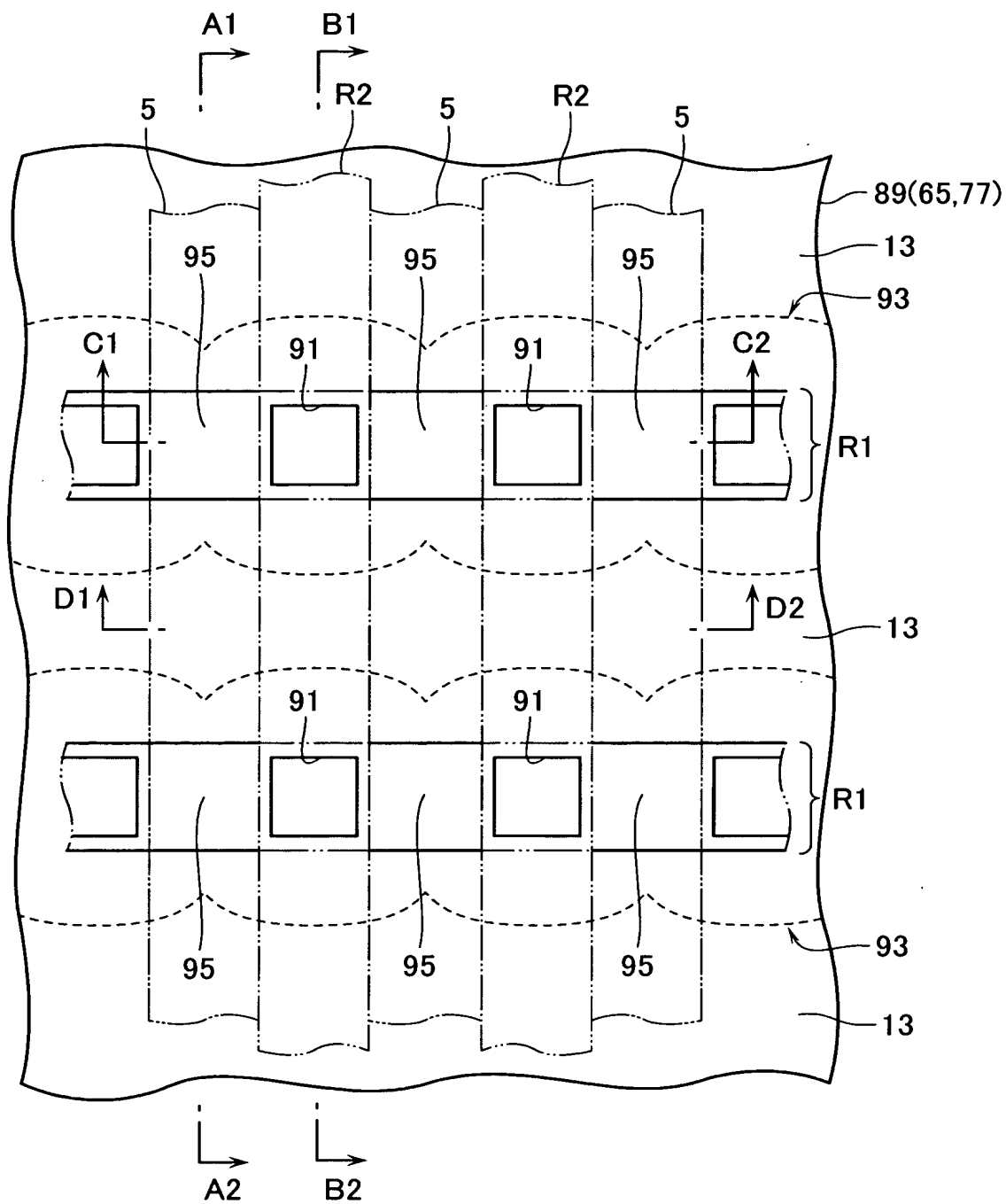


FIG. 32

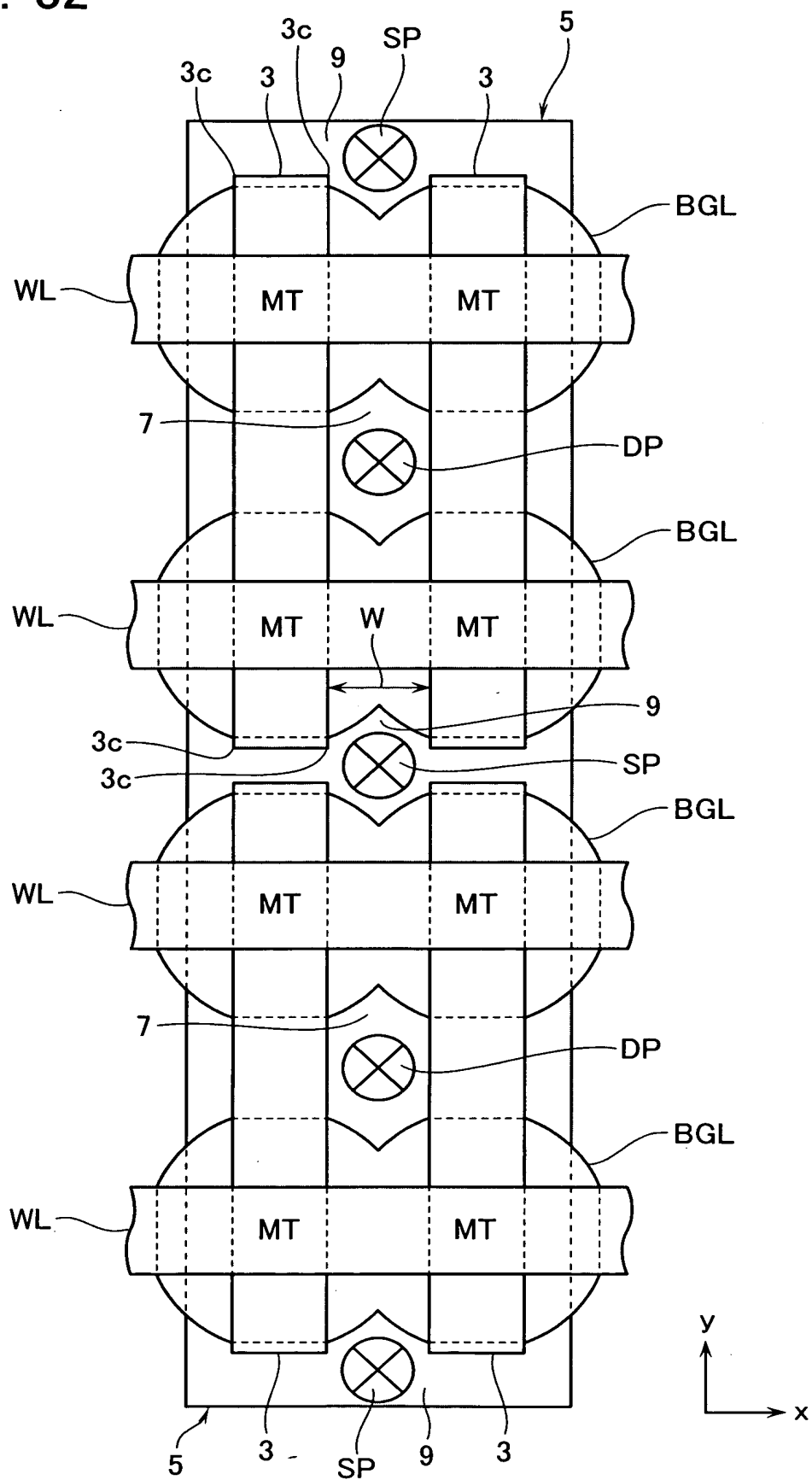
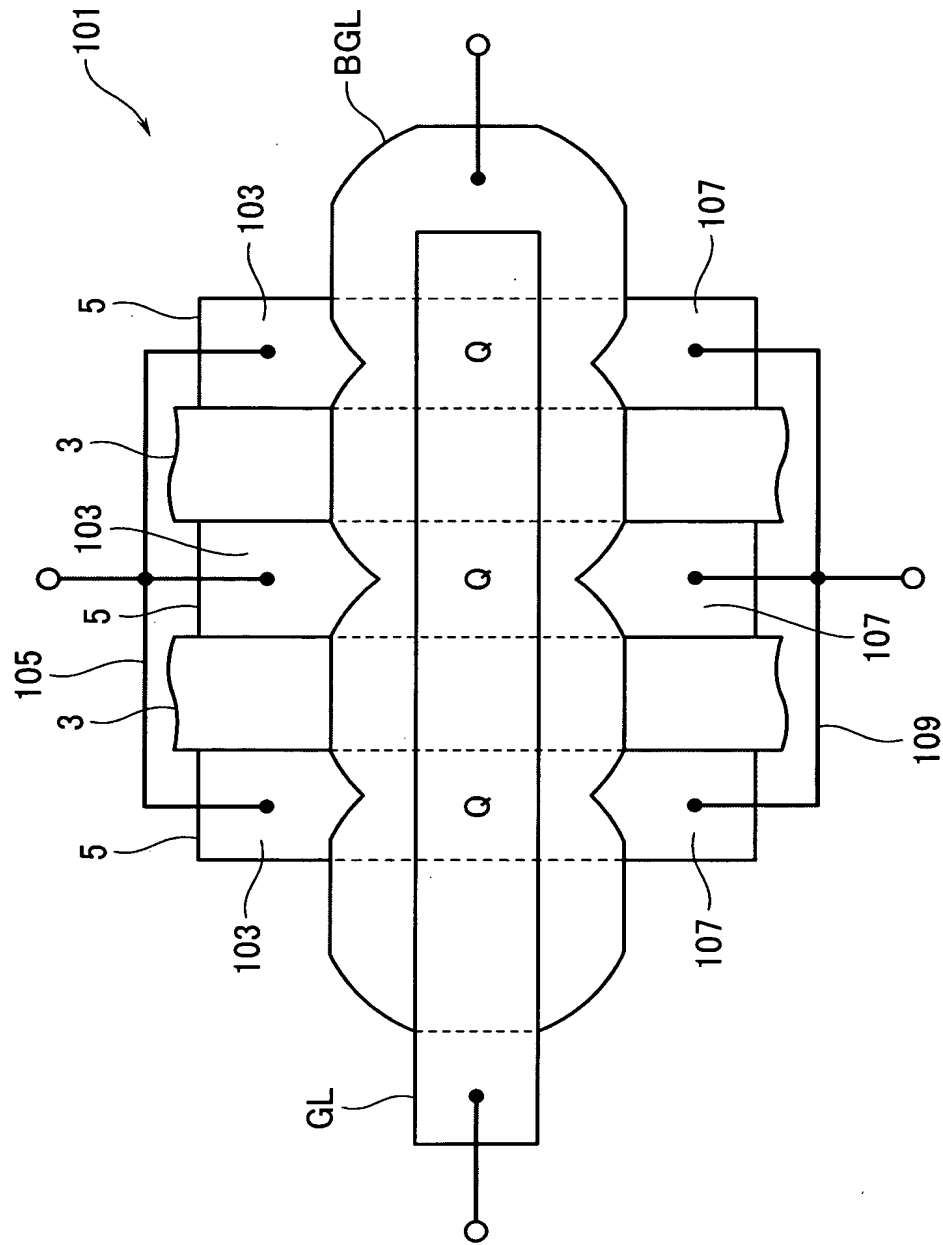




FIG. 33



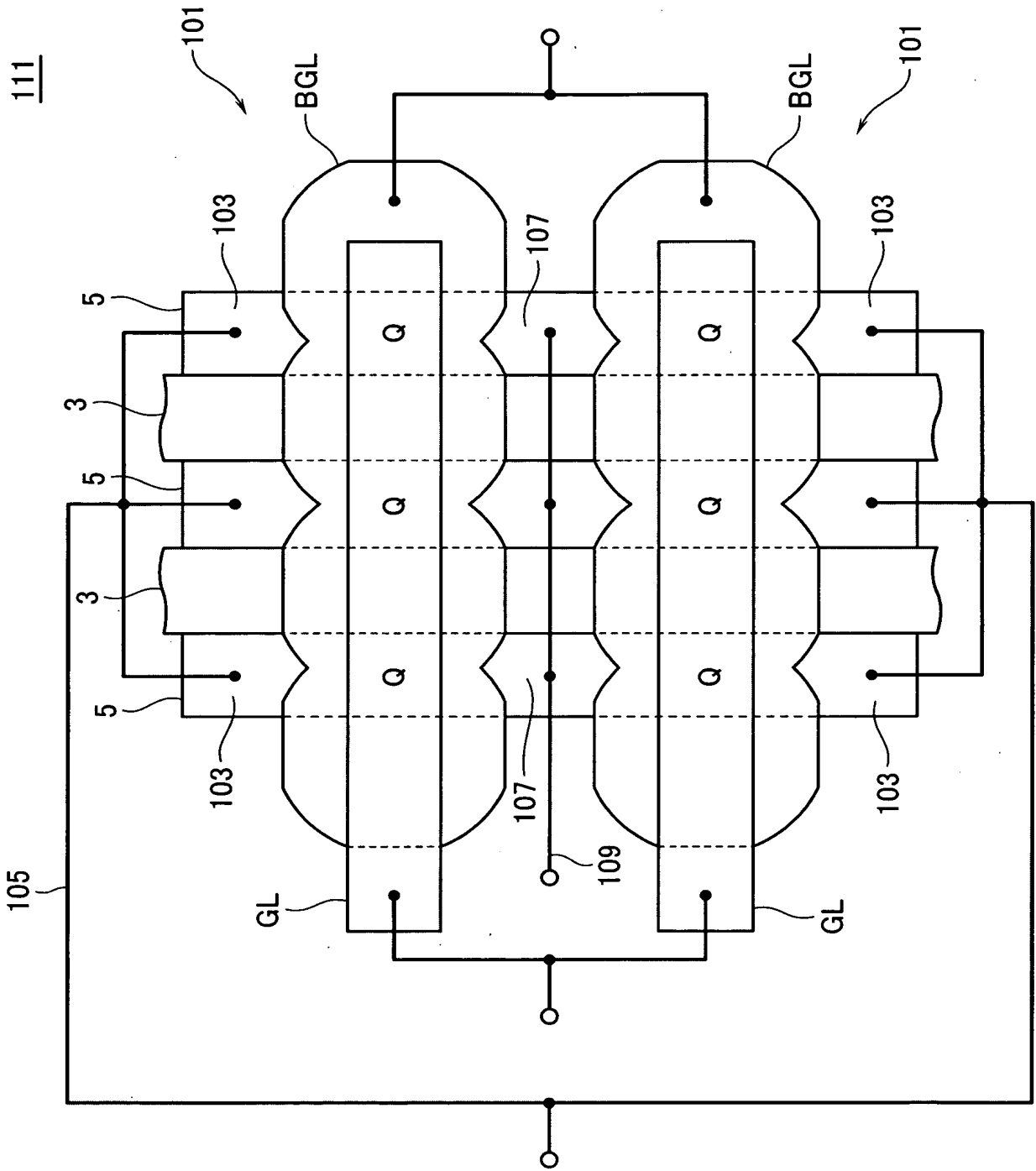


FIG. 34